

PATENT
Atty. Dkt. No. ROC920010210US1
MPS Ref. No.: IBMK10210

IN THE CLAIMS:

Please cancel claims 15-28 without prejudice, and amend the claims as follows:

1. (Currently Amended) An apparatus, ~~for adding at least two binary numbers, the two binary numbers each having at least 64 bits, the apparatus comprising:~~
~~a plurality of gates, the critical path through the plurality of gates being three gates configured to generate a sum of at least two binary numbers each having at least 64 bits.~~
2. (Original) The apparatus of claim 1 wherein:
at least one of the gates is a domino logic gate.
3. (Original) The apparatus of claim 1 wherein:
all the gates in the critical path are domino logic gates.
4. (Original) The apparatus of claim 3 wherein:
at least one of the domino logic gates in the critical path comprises a latch.
5. (Original) The apparatus of claim 4 wherein:
the latch is part of a scan path for testing the adder.
6. (Original) The apparatus of claim 3 wherein:
at least one of the domino logic gates comprises a multiplexer function.
7. (Original) The apparatus of claim 3 wherein:
at least one of the domino logic gates comprises a multiplexer function and a latch.
8. (Currently Amended) An apparatus, ~~for adding numbers with at least 64 bits, the apparatus comprising:~~

PATENT
Atty. Dkt. No. ROC920010210US1
MPS Ref. No.: IBMK10210

a critical path of three gate delays, the critical path comprising:

a first gate within a first level of logic, the first level of logic receiving at least two binary numbers, each with at least 64 bits, and generating multi-bit carry signals;

a second gate within a second level of logic, the second level of logic receiving the multi-bit carry signals and generating multi-bit section-based carry signals; and

a third gate within a third level of logic, the third level of logic receiving the multi-bit section-based carry signals and generating a sum of the received binary numbers.

9. (Original) The apparatus of claim 8 wherein:

the three gates are each a domino logic gate.

10. (Original) The apparatus of claim 9 wherein:

the domino logic gate in the first level of logic comprises a latch.

11. (Original) The apparatus of claim 10 wherein:

the latch is part of a scan path.

12. (Original) The apparatus of claim 9 wherein:

the domino logic gate in the first level of logic comprises a multiplexer function.

13. (Original) The apparatus of claim 9 wherein:

the first level of logic comprises:

a plurality of domino trees forming P, G, Z, and K carry signals; and
circuits forming multi-bit P, G, Z, and K carry signals;

the second level of logic comprises:

a plurality of domino trees forming section-based P, G, Z, and K carry signals; and

circuits forming multi-bit section-based P, G, Z, and K carry signals; and

PATENT
Atty. Dkt. No. ROC920010210US1
MPS Ref. No.: IBMK10210

the third level of logic comprises:

a plurality of domino logic gates forming sum bits.

14. (Currently Amended) An apparatus for adding numbers with at least 64 bits, the apparatus comprising:

a first level of logic for receiving at least two binary numbers and generating multi-bit carry signals, the first level of logic comprising domino logic gates;

a second level of logic receiving the multi-bit carry signals and generating multi-bit section-based carry signals, the second level of logic comprising domino logic gates; and

a third level of logic receiving the multi-bit section-based carry signals and generating a sum of the received binary numbers, the third level of logic comprising domino logic gates; wherein a longest circuit path through the apparatus is three domino logic gates.

15. (Canceled) The apparatus of claim 14 wherein:

the longest circuit path through the apparatus is three domino logic gates.

16. (Canceled) An apparatus for adding numbers, the apparatus comprising:

a first level of logic for receiving at least two binary numbers and generating multi-bit carry signals, the first level of logic comprising domino logic gates;

a second level of logic receiving the multi-bit carry signals and generating multi-bit section-based carry signals, the second level of logic comprising domino logic gates; and

a third level of logic receiving the multi-bit section-based carry signals and generating a sum of the received binary numbers, the third level of logic comprising domino logic gates.

17. (Canceled) The apparatus of claim 16 wherein:

the longest circuit path through the apparatus is three domino logic gates.

PATENT
Atty. Dkt. No. ROC920010210US1
MPS Ref. No.: IBMK10210

18. (Canceled) The apparatus of claim 16 wherein:
the longest circuit path through the apparatus is three domino logic gates plus an additional gate.
19. (Canceled) The apparatus of claim 16 wherein:
the longest circuit path through the apparatus is four domino logic gates.
20. (Canceled) The apparatus of claim 16 wherein:
the longest circuit path through the apparatus is five domino logic gates.
21. (Canceled) An apparatus for adding binary numbers, the apparatus comprising:
a first level of logic for receiving at least two binary numbers and generating multi-bit P, G, Z, and K carry signals, the first level of logic comprising:
a plurality of domino trees forming P, G, Z, and K carry signals; and
circuits forming the multi-bit P, G, Z, and K carry signals using the P, G, Z, and K carry signals;
a second level of logic receiving the multi-bit P, G, Z, and K carry signals and generating multi-bit section-based carry signals, the second level of logic comprising:
a plurality of domino trees forming section-based P, G, Z, and K carry signals using the multi-bit P, G, Z, and K carry signals; and
circuits forming multi-bit section-based P, G, Z, and K carry signals using the section-based P, G, Z, and K carry signals; and
a third level of logic receiving the multi-bit section-based carry signals and generating a sum of the received binary numbers, the third level of logic comprising:
a plurality of domino logic gates forming sum bits using the multi-bit section-based P, G, Z, and K carry signals.
22. (Canceled) The apparatus of claim 21 wherein:
the longest circuit path through the apparatus is three domino logic gates.
23. (Canceled) The apparatus of claim 21 wherein:

PATENT
Atty. Dkt. No. ROC920010210US1
MPS Ref. No.: IBMK10210

the longest circuit path through the apparatus is three domino logic gates and an additional gate.

24. (Canceled) The apparatus of claim 21 wherein:
the longest circuit path through the apparatus is four domino logic gates.
25. (Canceled) The apparatus of claim 21 wherein:
the longest circuit path through the apparatus is five domino logic gates.
26. (Canceled) A pipelined computational apparatus comprising:
an adder for adding at least two binary numbers, the two binary numbers each having at least 64 bits, the adder comprising a plurality of gates, the critical path through the plurality of gates being three gates.
27. (Canceled) The apparatus of claim 26 wherein:
at least some of the gates are domino logic gates.
28. (Canceled) The apparatus of claim 26 wherein:
all the gates in the critical path are domino logic gates.
29. (Currently Amended) An pipelined computational apparatus, comprising:
an adder for adding numbers with at least 56 bits, the adder comprising:
a critical path of three gate delays, the critical path comprising:
a first gate within a first level of logic, the first level of logic receiving at least two binary numbers and generating multi-bit carry signals;
a second gate within a second level of logic, the second level of logic receiving the multi-bit carry signals and generating multi-bit section-based carry signals; and
a third gate within a third level of logic, the third level of logic receiving the multi-bit section-based carry signals and generating a sum of the received binary numbers.

PATENT

Atty. Dkt No. ROC920010210US1
MPS Ref. No.: IBMK10210

30. (Original) The apparatus of claim 29 wherein:
the three gates are each a domino logic gate.